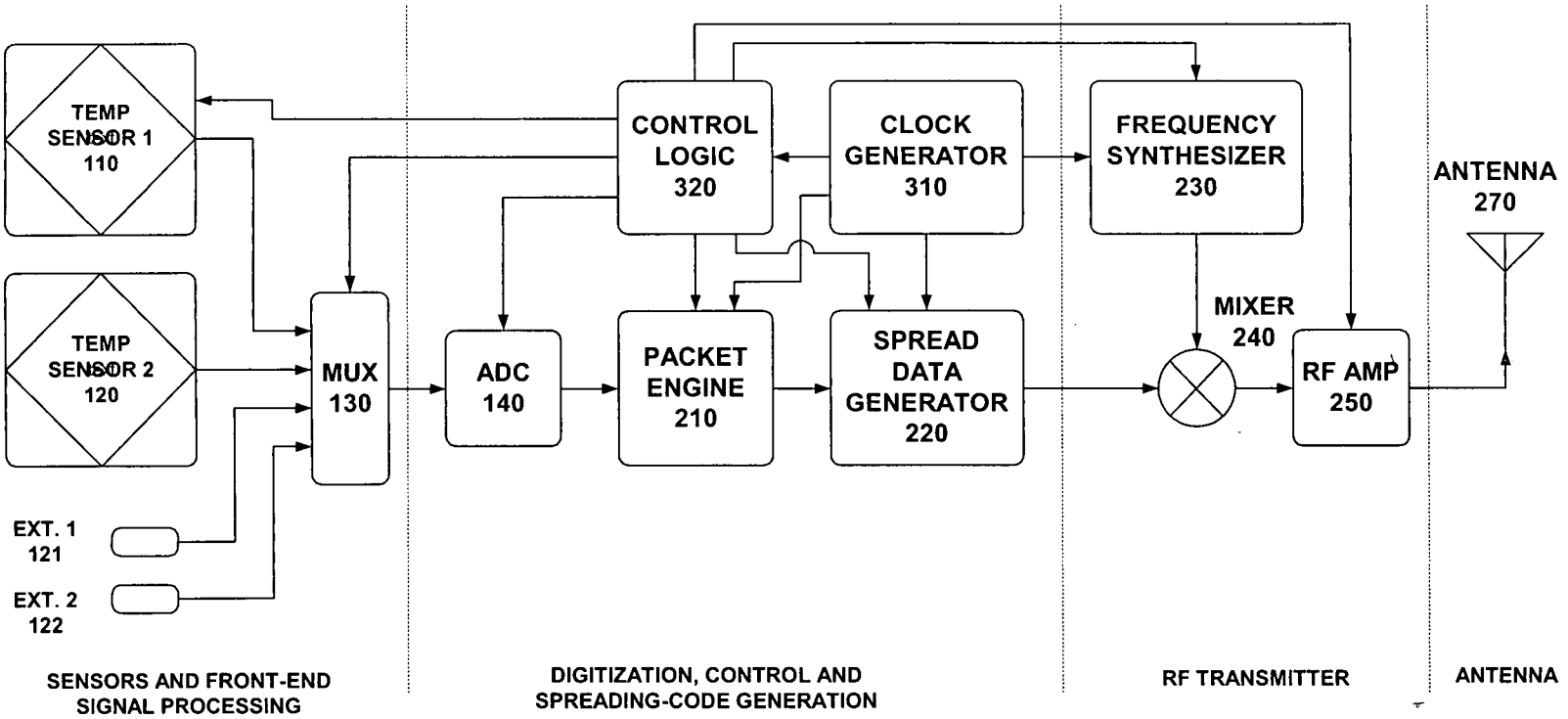


Fig. 1

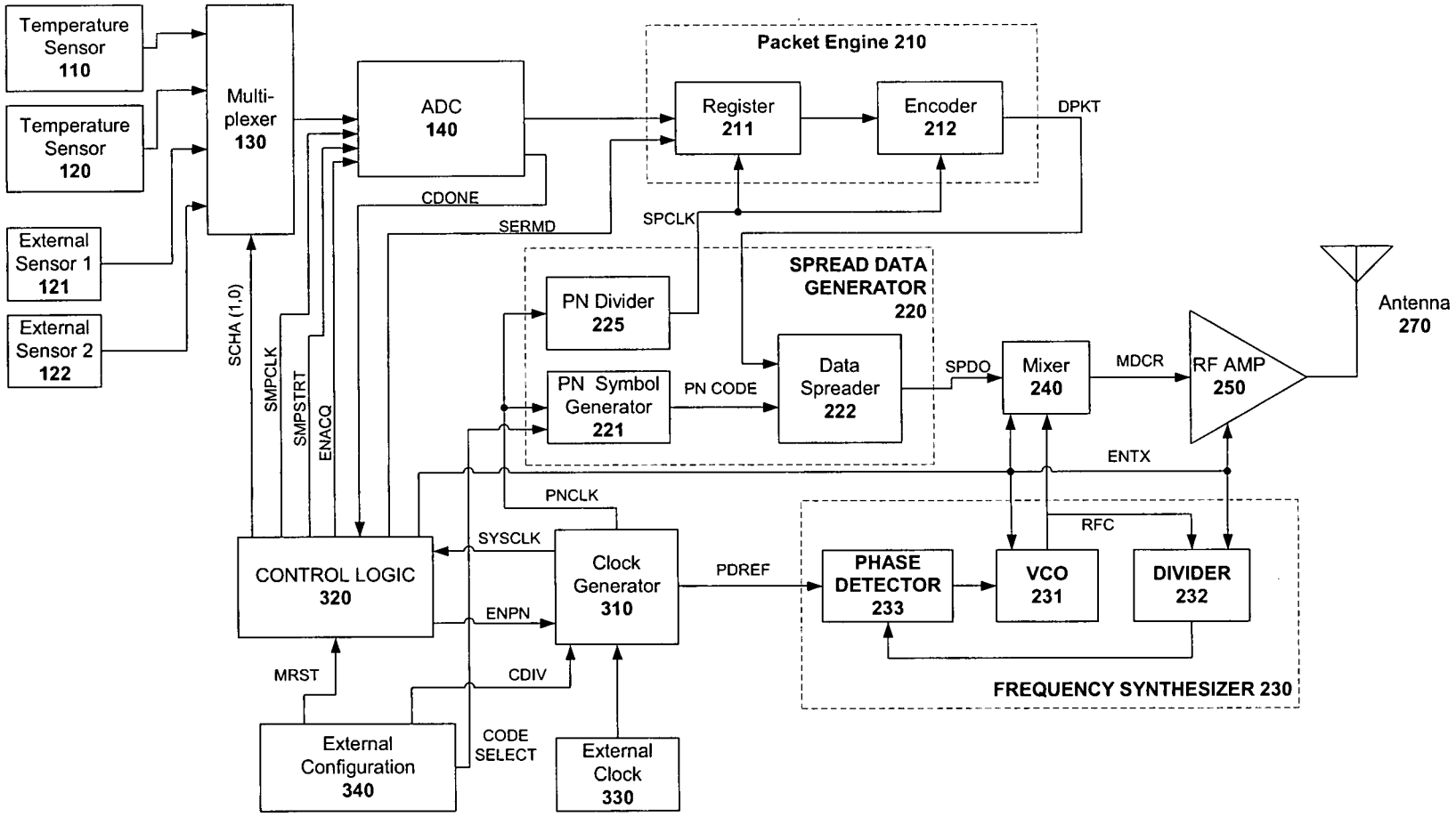
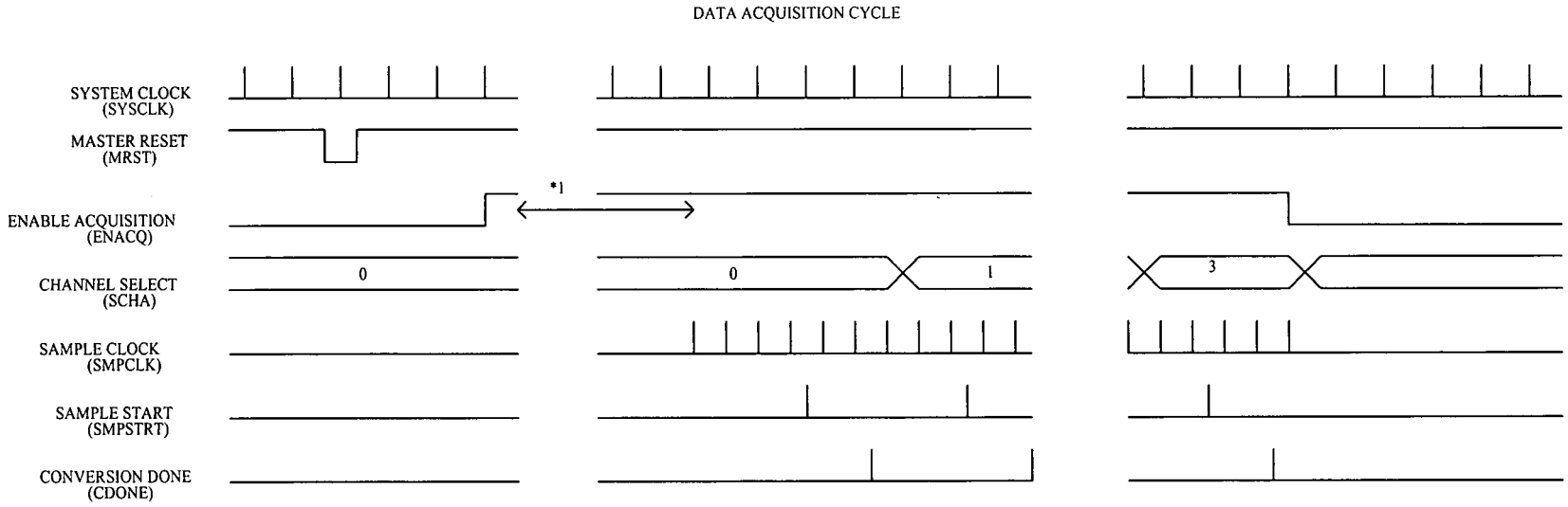
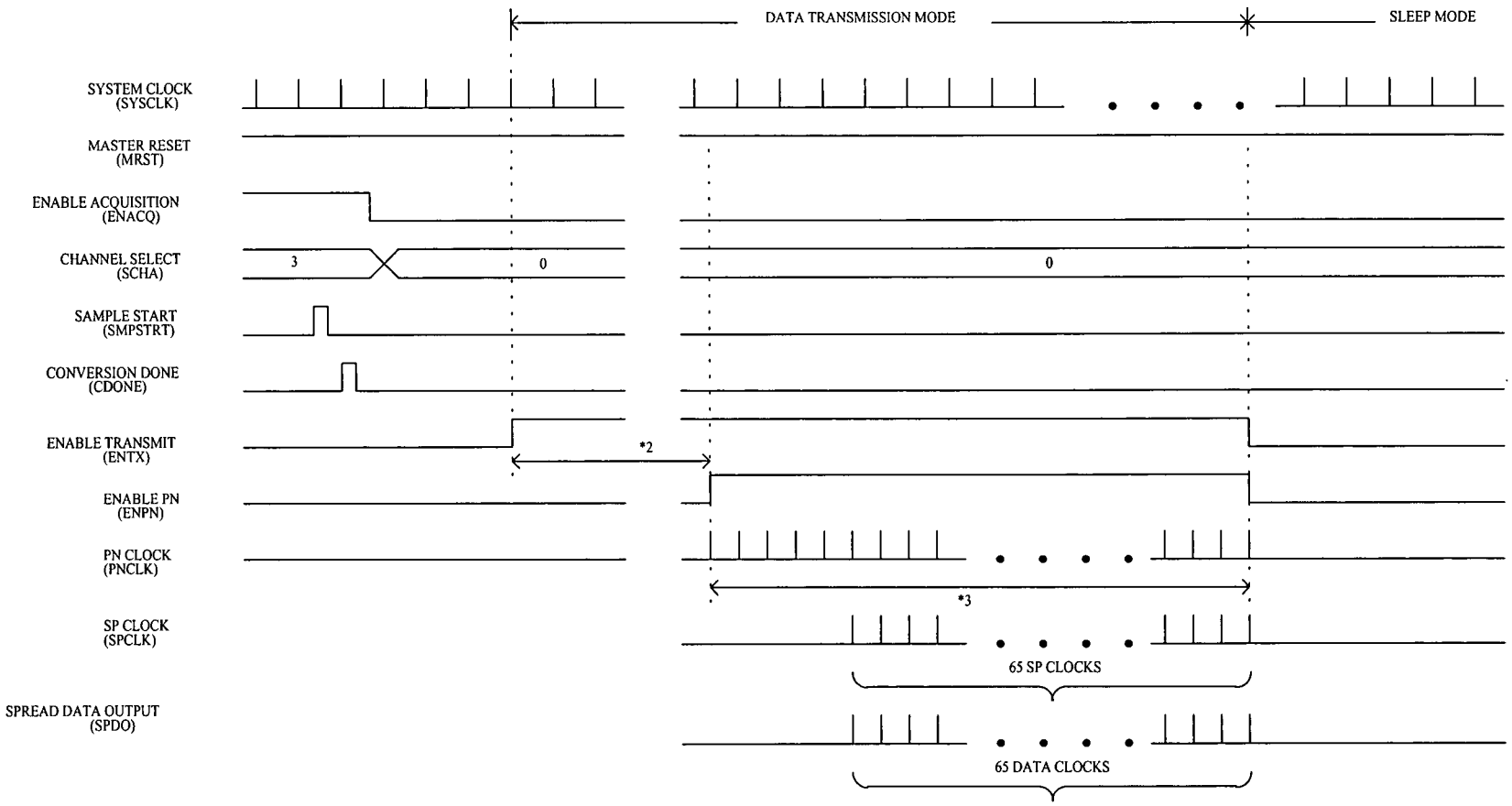


Fig. 2



*1 There are 1024 system clock cycles between enable acquisition and the beginning of the sample clock. This wait period is for acquisition component stability.

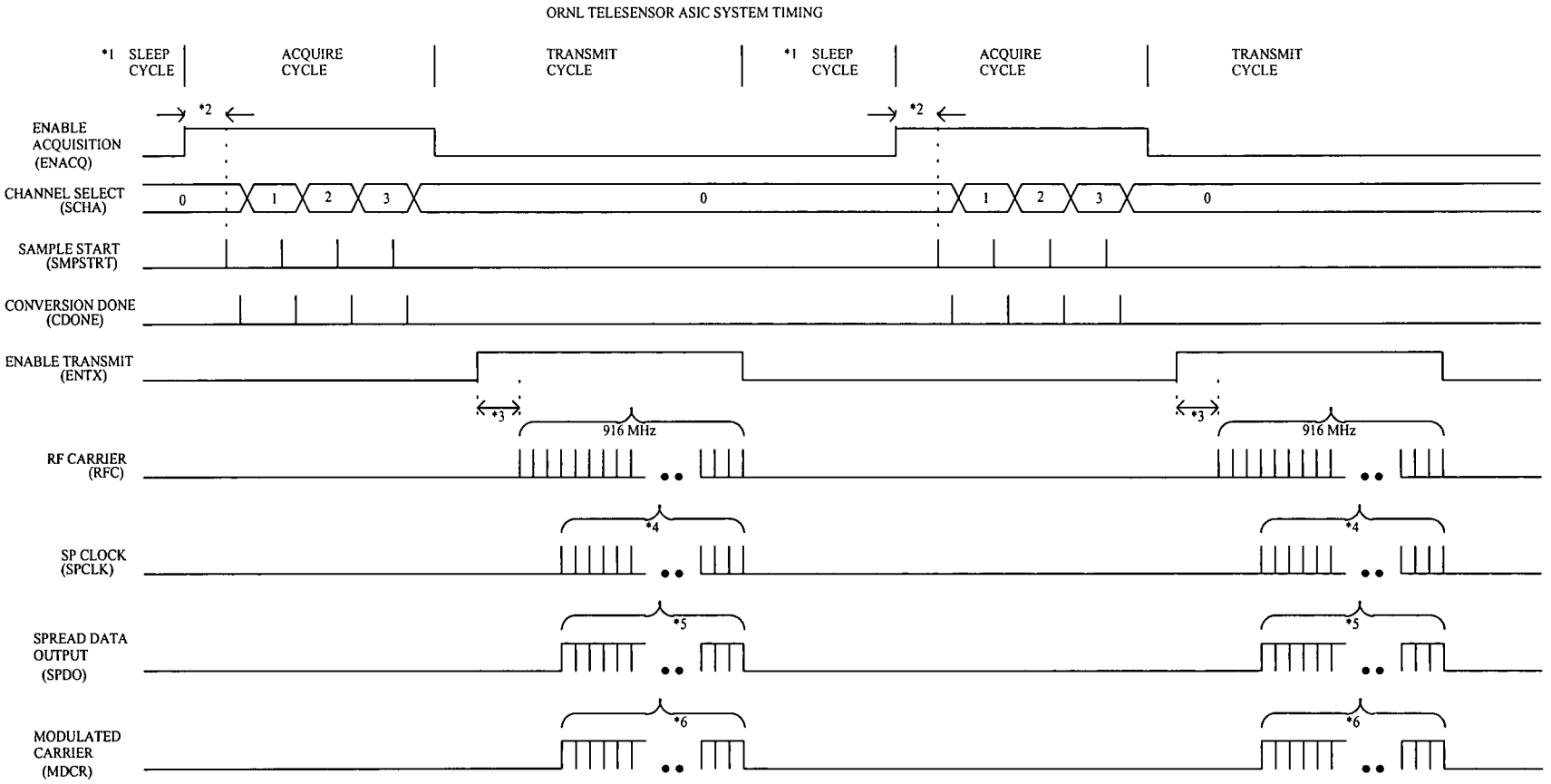
Fig. 3



*2 There are 1024 system clock cycles between enable transmit and the beginning of the transmit (PN) clock. This wait period is for transmit component stability.

*3 The SP clock is the PN clock divided by 53.

Fig. 4



*1 Selectable to 8 s, 1 s, 0.125 s, or 0 (based on system clock).

*2 Time is 1024 system clocks (acquire stability).

*3 Time is 1024 system clocks (transmit stability).

*4 Spread (SP) clock is PN clock divided by 63.

*5 Spread data = (serial data) XOR (encryption PN code)

*6 Data packet = (spread output) XOR (rf carrier)

Fig. 5

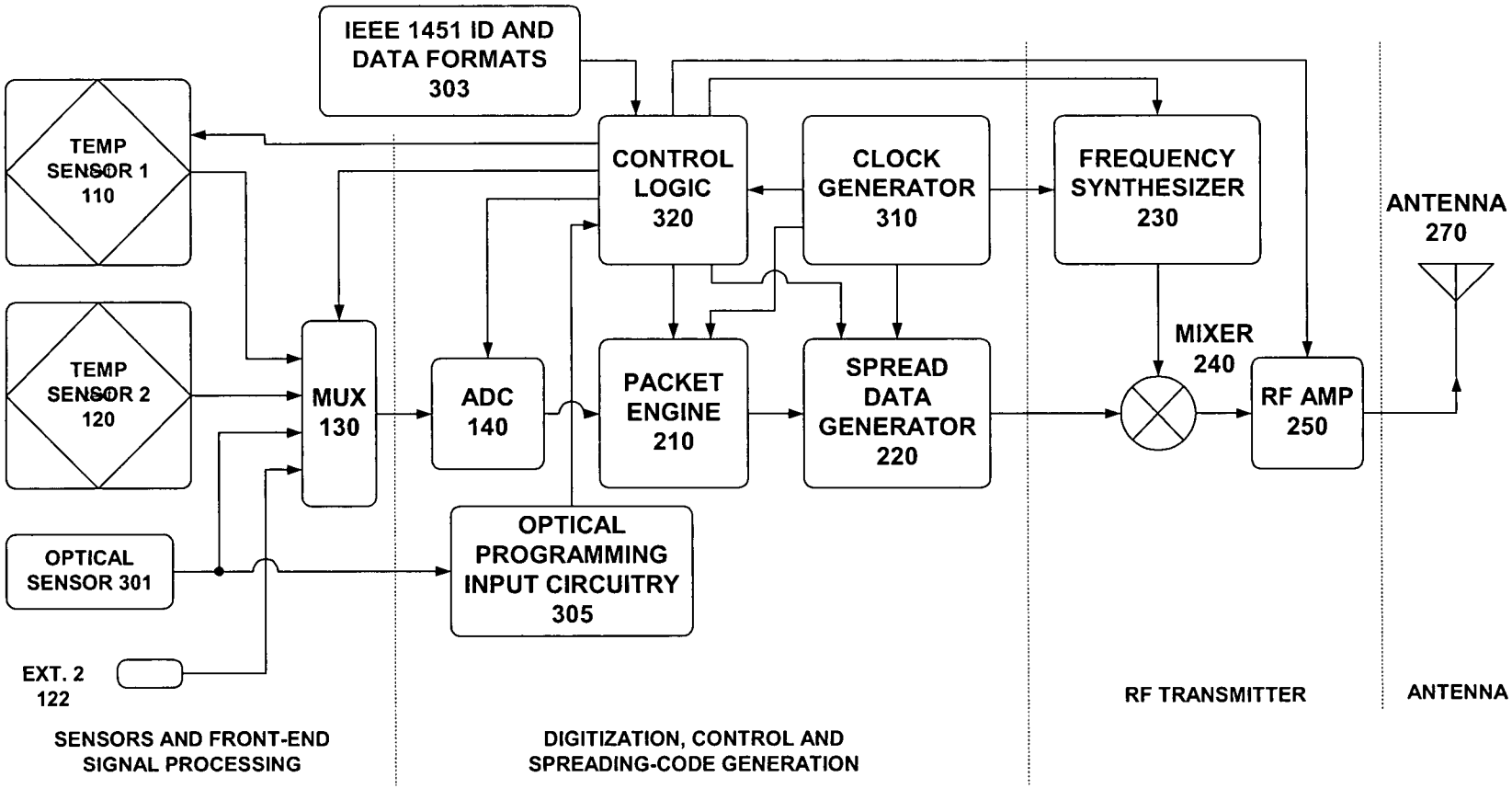


Fig. 6

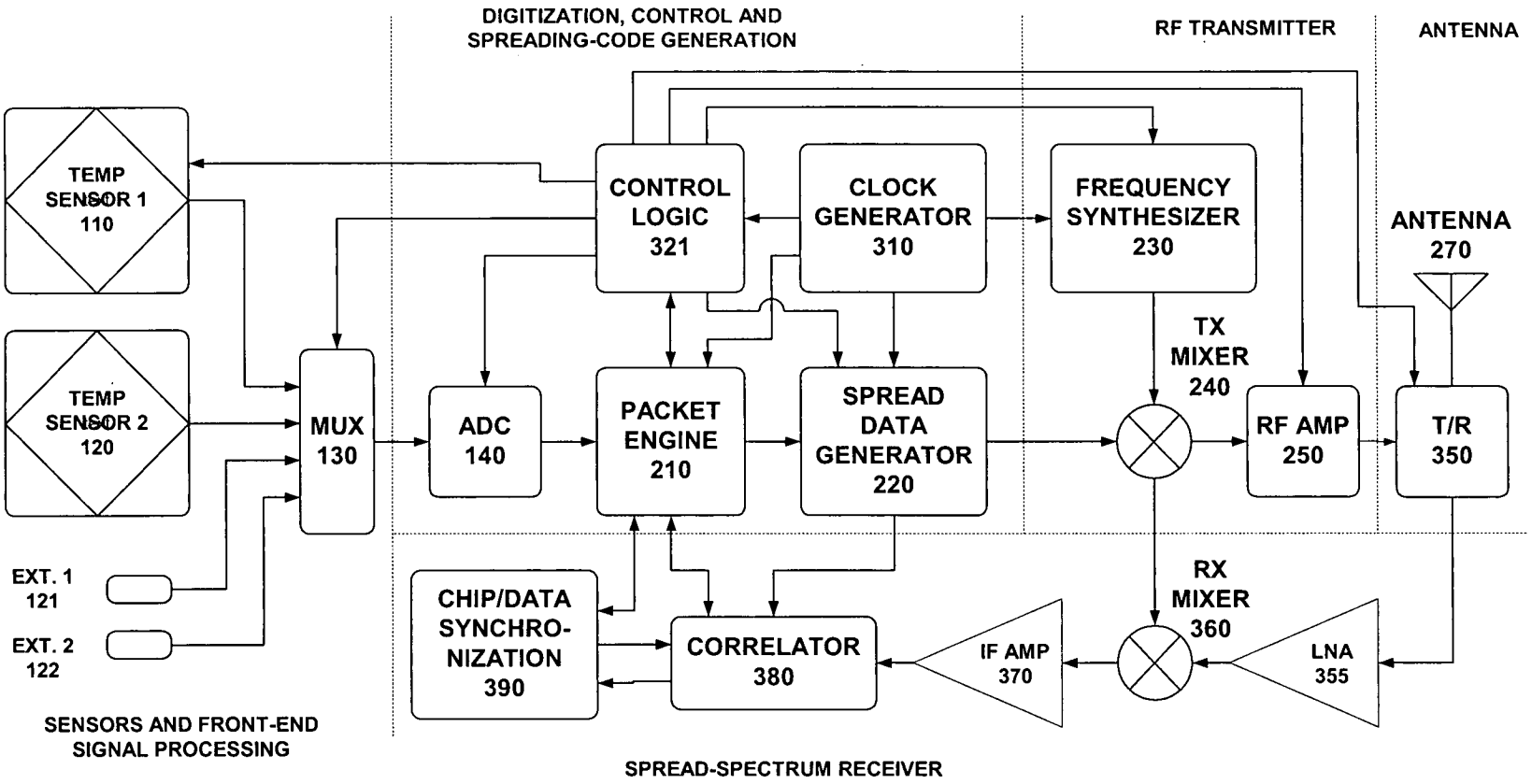


Fig. 7

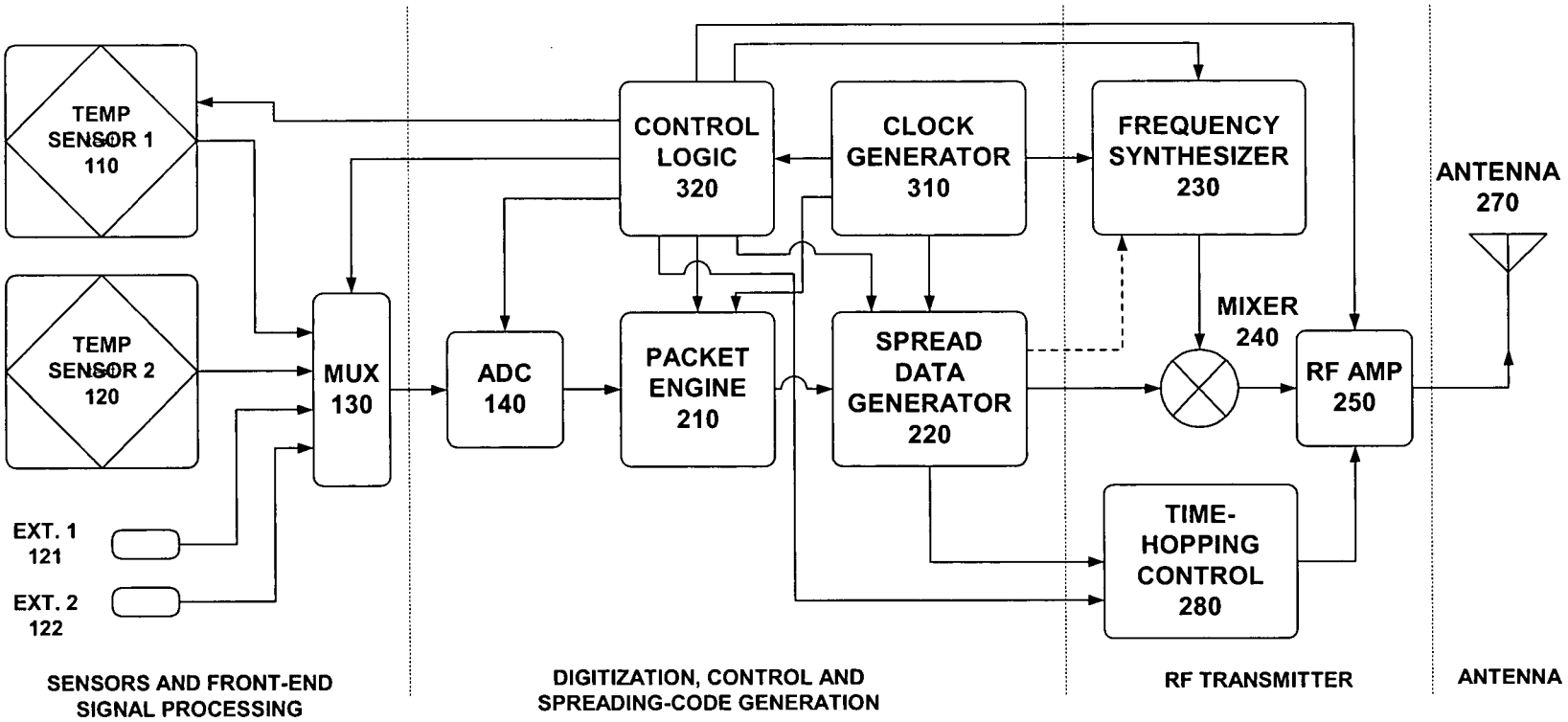


Fig. 8

ORNL Wireless Temperature Telesensor Chip

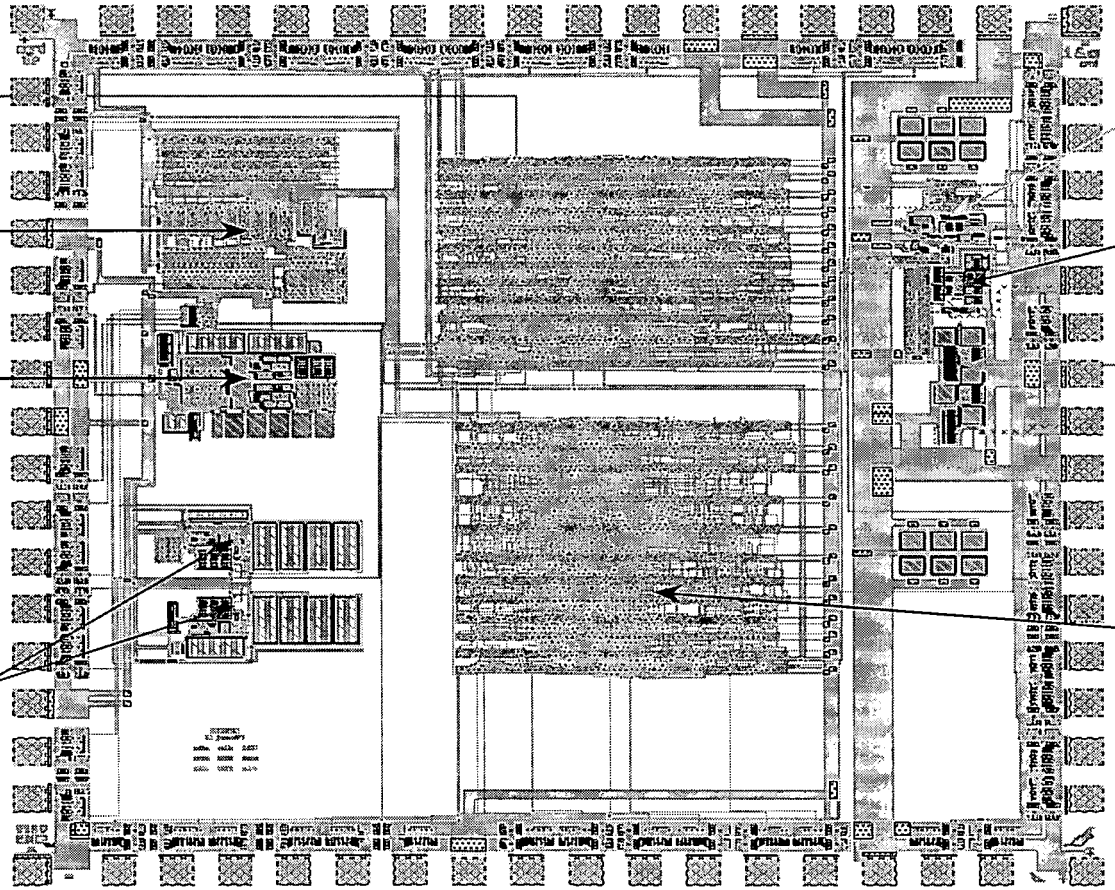


Fig. 9

Advanced Wireless Telesensor Chip

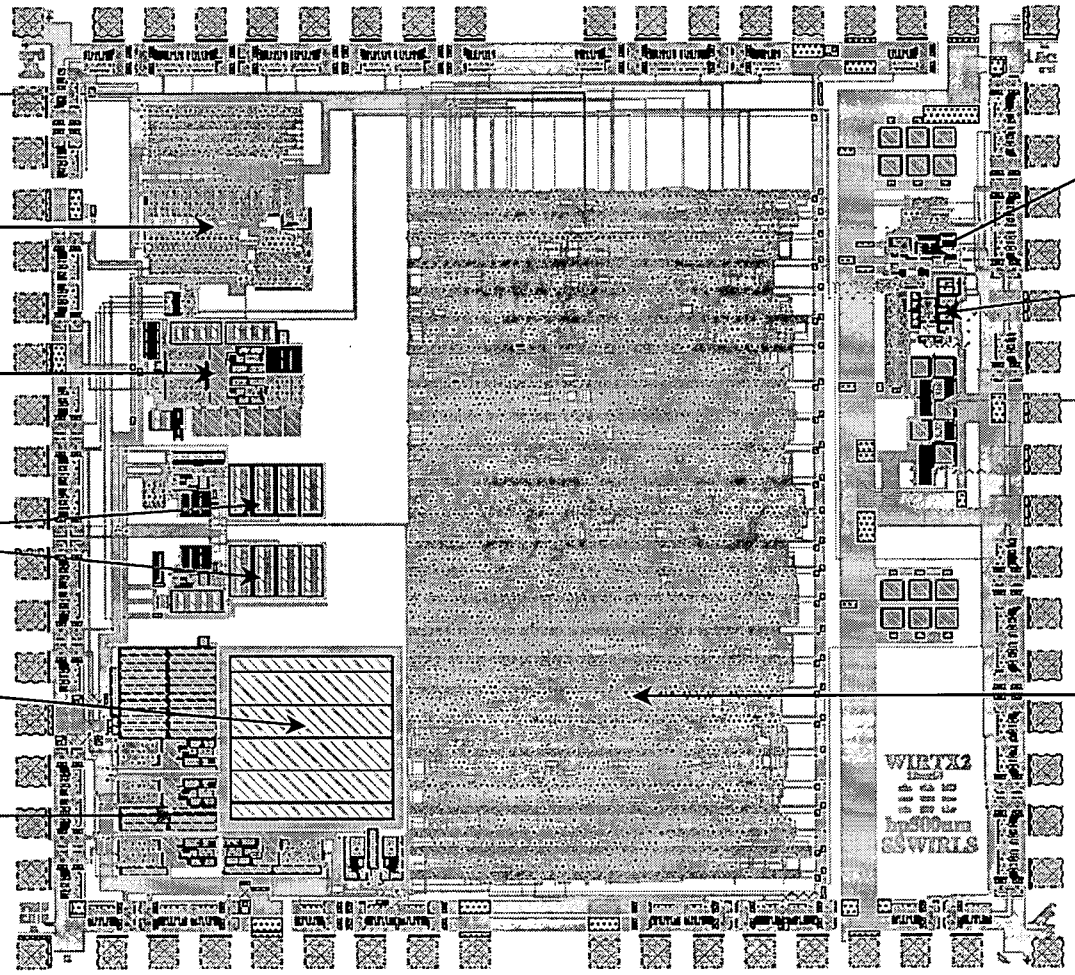


Fig. 10